URN etd-0407109-183725-2110
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Statistics This thesis had been viewed 49 times. Download 74 times.
Department
Year 2001
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title A successive approximation ADC based on a new segmented DAC
Date of Defense 0000-00-00
Page Count 47

Keyword
successive approximation ADC
segmented DAC
current-mode DAC

Abstract
A successive approximation analog-to-digital converter (ADC) based on a new segmented digital-to-analog converter (DAC) architecture is presented. A more efficient method which is the bi-direction segmented current-mode approach is proposed to implement the high-resolution and high speed DAC. This DAC has the maximum integral nonlinearity (INL) error of 0.47 LSB, and the maximum differential nonlinearity (DNL) error of 0.154 LSB. Based on this new DAC, a 3-V, 8-bit, 2-MS/s ADC is realized. The whole circuit is implemented by the TSMC 1P4M 0.35μm CMOS process. The experimental results show that the INL of ADC is less than 0.82 LSB. Meanwhile, the DNL is less than 0.31 LSB. The power consumption is only 2.6mW with the effective number of bits of 7.
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Files etd-0407109-183725-2110-001.pdf

indicate access worldwide
Date of Submission 2002-08-21